REMARKS

The Examiner's Remarks with respect to Election/Restrictions have been noted. Claims 8-17 have been withdrawn from consideration.

The indication of Allowability of claims 6 and 7 if rewritten in independent form to include all of the limitations of the base claims and any intervening claims has been noted with appreciation. Original claim 6 has been rewritten as new independent claim 18 to include all of the limitations of original base claim 1 and intervening claim 2. Accordingly, claim 18 is believed to be in condition for allowance.

Original Claim 7 has been amended to depend from new claim 18 and to include minor editorial changes. Accordingly, claim 7 is believed to be in condition for allowance.

Claims 1 and 4 have been amended in order to overcome the informalities noted by the Examiner. In addition, claims 1-5 have been amended in order to better define the invention and bring the language of these claims more closely into conformity.

Paragraph 0042 of the specification has been amended to correct a typographical error which went un-noted prior to filing.

Claim Rejections 35 USC § 102

Original Claim 1 has been rejected as anticipated by Admitted Prior Art, referred to as "Admission", which appears on page 2, lines 6-11 of Applicant's published specification.

The Examiner refers to element 23 shown in Figure 3 of the drawings. Figure 3 illustrates a bi-directional pin of an IC that has BSR access to control of a pin, and a tri-stating signal that can simultaneously tristate all pin outputs. The referenced description on page 2 briefly describes a slight modification that can be made to the BSR-controlled pad driver to permit implementation of a HIGHZ instruction defined by 1149.1. However, Admission does not describe a tristate control circuit for selectively controlling the pin driver enable input of pin drivers that is responsive to a control input for temporarily de-asserting a signal that tri-states pin drivers during a capture cycle of a TAP in which pin logic values are captured by the BSR.

Amended claim 1 calls for "a tristate pin driver that can be enabled by the "BSR unless a tristate control signal from said TAP controller is asserted; a first mode control input signal; and a tristate control circuit that, when said first mode control input signal is logic 1, temporarily de-asserts said tristate control signal during a capture state of said TAP controller in which pin logic values are captured by the BSR" (emphasis added). These features are neither taught nor remotely suggested by Admission. Reconsideration is respectfully requested.

Original claim 1 has also been rejected under 35 U.S.C. 102(b) as being anticipated by Levitt (US Patent No. 5,513,186).

The Circuit of Levitt disables the pin driver for the entire duration of a boundary scan test. The present invention disables the pin driver for the duration of a boundary scan test, but, contrary to Levitt, temporarily permits the BSR to enable the pin driver during the capture state.

The circuit of Levitt directly controls the enable input of the pin driver. In the present invention, the BSR directly controls the enable of the pin driver unless, as indicated above, the tristate control from the TAP controller overrides to force the pin driver to be disabled; the forcing action can be temporarily de-asserted during the capture state. Levitt does not disclose any means for temporarily enabling the pin driver while in test mode or while pin logic values are captured. Levitt Figures 6 and 7 show that pins are tristated, then pin values are captured, then it returns to normal functionality. Also, Levitt cannot test the tristate pin driver because it is always disabled during boundary scan test. The primary objective of Levitt is to "avoid degradation of speed of operation during normal operation", therefore, it would not be obvious to use any aspect of that invention to overcome the problems which faced Applicant, i.e., for "testing the enable function" of a tristate driver and testing for inadvertent short circuits "without causing excessive current". Reconsideration is respectfully requested.

Claim Rejections - 35 USC § 103

Claims 2 and 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Admission in view of Nadeau-Dostie et al (U.S. Patent No. 6,000,051, referred to as Nadeau-Dostie).

As indicated earlier, Admission neither teaches nor suggests the present invention.

The circuit of Nadeau-Dostie updates the update latch (item 70 in Nadeau-Dostie Figures 4 and 7) during the Update-DR state, but that latch is not used during high-speed test mode when IBIST is logic 1. In the present invention, the update latch is used, but is not updated during the Update-DR state – instead, it is updated later during the Run-test/Idle or Select-DR state. This is not an obvious change to make, especially since the primary objective of Nadeau-Dostie is "testing high speed interconnectivity", whereas the primary objective of the present invention is "testing the enable function" of a tristate driver and testing for inadvertent short circuits "without causing excessive current".

Accordingly, the combination of Admission and Nadeau-Dostie fails to teach or even remotely suggest the invention of claim 1 and its dependent claims. Reconsideration is respectfully requested.

Claims 4 and 5 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Admission in view of Jacobson (US Pat. 6,499,124).

As indicated earlier, Admission neither teaches nor suggests the present invention.

Jacobson discloses a circuit that uses a security bit that is permanently set in non-volatile memory to a logic value that prevents boundary scan data from arriving at its destination along a specific path, which may be the enable path to a tristate driver, to "thwart a would-be pirate" from accessing the data (in INTEST mode). There is no means for disabling a pin driver during boundary scan test (EXTEST mode) and temporarily permitting enabling the pin driver during a capture state of the TAP controller. The primary objective of Jacobson is to provide a "security circuit", therefore it would not be obvious to use any aspect of Jacobson for "testing the enable function" of a tristate driver and testing for inadvertent short circuits "without causing excessive current".

Accordingly, the combination of Admission and Jacobson fails to teach or even remotely suggest the invention of claim 1 and its dependent claims. Reconsideration is respectfully requested.

In view of the foregoing, it is believed that the claims under consideration clearly patentably distinguish over the applied references, taken singly or in any combination. Applicant respectfully submits that the application is in condition for allowance. Early favorable reconsideration is respectfully requested.

Respectfully Submitted,

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